WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a portion disposed on the semiconductor layer;

a passivation layer formed on the data line and having a first contact hole exposing at least a portion of a boundary of the gate line or the data line; and

a contact assistant formed on the passivation layer and on the exposed portion of the boundary of the gate line or the data line.

2. The thin film transistor array panel of claim 1, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo or Mo alloy and an upper film of Al or Al alloy.

3. The thin film transistor array panel of claim 2, wherein the contact assistant is in contact with the lower film.

4. The thin film transistor array panel of claim 4, wherein the contact assistant comprises ITO or IZO.

5. The thin film transistor array panel of claim 5, further comprising:

a drain electrode separated from the data line and formed on the gate insulating layer and the semiconductor layer; and

a pixel electrode formed on the passivation layer and connected to the drain electrode through a second contact hole.

6. An exposure mask comprising:

an opaque area blocking light; and

a slit pattern formed in the opaque area and including a plurality of slits,

wherein the slits are substantially rectilinear, and width of each slit and distance between the slits are in a range about 0.8-2.0 microns.

7. The mask of claim 6, wherein the slits have depressions.

8. The mask of claim 6, wherein the mask is utilized in manufacturing a thin film transistor panel including a display area where a plurality of signal lines intersect each other and a peripheral area where end portions of the signal lines are

disposed, the slits include first slits in the display area and second slits in the peripheral area, and the first and the second slits have different width and distance.

9. The mask of claim 6, wherein the mask is utilized in manufacturing a thin film transistor panel including a display area where images are displayed and a peripheral area around the display area, the slits include first slits in the display area and in the peripheral area and second slits in a remaining area, and the first and the second slits have different width and distance.

10. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate line on an insulating substrate;

forming a gate insulating layer;

forming a semiconductor member;

forming a data conductive layer including a data line and a drain electrode;

forming a passivation layer having a contact hole exposing at least a portion of the drain electrode and a portion of the gate insulating layer near an edge of the drain electrode; and

forming a pixel electrode connected to the drain electrode through the contact hole,

wherein at least one of the semiconductor member and the passivation layer is patterned by photolithography using a mask having a plurality of substantially rectilinear slits and width of each slit and distance between the slits range from about 0.8 to about 2.0 microns.

11. The method of claim 10, wherein the mask comprises a first area blocking light, a second area provided with the slits for partially transmitting light, and a third area fully transmitting light.

12. The method of claim 11, wherein the photolithography forms a positive photoresist including a first portion on the data line and a first portion of the drain electrode, a second portion on a second portion of the drain electrode, and a third portion on an end portion of the gate line, the second portion of the photoresist is thinner than the first portion of the photoresist, and the third portion of the photoresist is thinner than the second portions of the photoresist.

13. The method of claim 12, wherein the photoresist further comprises a fourth portion on an end portion of the data line and having a thickness smaller than the first portion of the photoresist.

14. The method of claim 13, further comprising:

performing etching using the photoresist to expose portions of the passivation layer under the second and the fourth portions of the photoresist and a portion of the gate insulating layer under the third portion; and

removing the exposed portions of the passivation layer and the gate insulating layer to form contact holes exposing the end portions of the gate line and the data line.

15. The method of claim 14, wherein the slits include first slits corresponding to the second portion of the photoresist and second slits corresponding to the fourth portion of the photoresist, and the first and the second slits have different width and distance.

16. The method of claim 13, wherein the patterning of at least one of the semiconductor member and the passivation layer by photolithography comprises:

depositing a semiconductor layer on the gate insulating layer;

depositing an insulating layer on the data conductive layer;

forming the photoresist on the insulating layer;

performing etching using the photoresist to expose portions of the passivation layer under the second and the fourth portions of the photoresist and a portion of the gate insulating layer under the third portion;

removing the exposed portions of the passivation layer and the gate insulating layer to form contact holes exposing the end portions of the gate line and the data line and to expose portions of the semiconductor layer; and

removing the exposed portions of the semiconductor layer to form the semiconductor member.

17. The method of claim 16, wherein the semiconductor member comprises a plurality of semiconductor portions separated from each other at positions between adjacent data lines.

18. The method of claim 16, wherein the thin film transistor panel includes a display area where the gate line intersects the data line and a peripheral area

where end portions of the gate line and the data line are disposed, the slits include first slits in the display area and in the peripheral area and second slits in a remaining area, and the first and the second slits have different width and distance.

19. The method of claim 10, wherein at least one of the gate line and the data conductive layer comprises a lower film of Cr, Mo or Mo alloy and an upper film of Al or Al alloy.

20. The method of claim 19, wherein the drain electrode comprises the lower film and the upper film and the method further comprises:

removing the upper film of the at least a portion of the drain electrode before forming the pixel electrode.

21. The method of claim 10, wherein the mask is aligned such that at least one of the slits overlaps a boundary of the drain electrode.

22. The method of claim 21, wherein the at least one of the slits has a depression.

23. The method of claim 10, wherein the mask is aligned such that at least two of the slits are disposed out of the drain electrode.